REMARKS

Claims 1-31 are pending in the present application. In the Office Action mailed November 03, 2005, the Examiner rejected claims 1, 2, 4, 17-19, and 24 under 35 U.S.C. §103(a) as being unpatentable over Ikeda et al. (USP 6,507,004) taken with Shikata et al. (USP 6,051,806). The Examiner next rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Ikeda et al. taken with Shikata et al., as applied to claims 1, 2, 4, 17-19, 22, and 24 above, and further in view of Hedberg (USP 6,713,708). Claims 5 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ikeda et al. taken with Shikata et al as applied to claims 1, 2, 4, 17-19, 22, and 24 above, and further in view of Kroll (USP 4,5080,954). Claims 6 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ikeda et al. taken with Shikata et al as applied to claims 1, 2, 4, 17-19, 22, and 24 above, and further in view of Church et al. (USP 6,177,645). Claim 23 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ikeda et al. taken with Shikata et al as applied to claims 1, 2, 4, 17-19, 22, and 24 above, and further in view of Ulrich (USP 6,236,014).

Claims 7-16, 20, and 25-31 have been canceled.

Applicant has amended claim 1 to further define the power source as comprising an inverter controller operably connected to the inverter that receives feedback regarding a weld state at a weld and controls the inverter to provide a welding output at a current level greater than the rated current level of the power source when a short is detected to clear the short. The Examiner rejected claim 1 as being unpatentable over the combination of Ikeda et al. and Shikata et al.

Ikeda et al. discloses a DC power supply for arc utilizing apparatuses that is capable of providing a constant current power for welding based on a series of inputs of differing voltages. In this regard, the reference discloses an inverter that conditions a raw power input into a form usable for arc welding or other arc related process. To effectuate a desired output voltage in light of the variability in input voltage, Ikeda et al. discloses a controller that selectively biases either a thyristor or a voltage-lowering converter. In this regard, the reference discloses a system that measures a voltage between input terminals of a power supply and, based on the measured voltage, either turns on a thyristor or a voltage-lowering converter so that a desired weld voltage is delivered. That is, "When a 100 V level voltage is applied between the power supply input terminals, the thyristor is turned on, the voltage-lowering converter is turned off and the switch is circuit is turned on." Ikeda et al., Abstract. "When one of the 200 V level voltages is connected, the thyristor is turned on, the voltage-lowering converter is turned off, and the switch circuit is

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turned off." Id. On the other hand, "When one of the 400 V level voltages or the 575 V voltage is applied between the power supply input terminals, the thyristor is turned off, the voltage-lowering converter is turned on, and the switch is turned off." Id.

The Examiner also relied upon Shikata et al. in rejecting claim 1. The Examiner relied upon Shikata et al. for its teaching of a MIG welding with an inverter. However, as set forth below, like Ikeda et al, Shikata et al. fails to teach or suggest that called for in claim 1.

As referenced above, claim 1 has been amended to clarify that the claimed inverter is controlled by an inverter control to provide an output current greater than a rated current when a short is detected at a weld to clear the short at the weld. Neither Ikeda et al. nor Shikata et al. makes such a teaching.

Ikeda et al. discloses a system to allow a power source to provide a desired output despite variability in a power input. Shikata et al. discloses a MIG welder having an inverter, but no teaching that the MIG welder is operable with a 115V input. Neither reference discloses or suggests an invertor that provides a greater-than-rated output current to clear a detected short. As such, it is believed that claim 1 is patentably distinct from that taught and/or suggested by the art.

Claim 17 has been amended to incorporate, in part, the subject matter of claim 20. Claim 20 was rejected based on the combination of Ikeda et al., Shikata et al., and Church. The Examiner relied on Church for teaching of a power factor correction circuit. However, claim 17 (as well as claim 6) have been amended to further define the power factor circuit as being configured to boost an input to a voltage level greater than 115V. Church explicitly teaches "a buck converter 20 [which] is used as a power factor correcting circuit (PFC) to create an intermediate voltage in the range of 100-150 volts, preferably, 130 volts, across output storage capacitor 30, as shown in FIG. 2," for "input voltages in the range of 200-600 VAC with a smooth output voltage below 113 volts." Church, col. 6, ll. 57-61 and col. 4, ll. 6-8. In fact, Church teaches away from a boost converter in stating that "a boost power factor correcting circuit is not applicable for use in the present invention." Id., col. 3, ll. 11-12. As such, Church explicitly teaches away from that being called for in claims 6 and 17. Therefore, one skilled in the art would not be motivated to combine Ikeda et al., Shikata et al., and Church in a manner suggested by the Examiner. Accordingly, claims 6 and 17 are also believed to be in condition for allowance.

Regarding the rejections of claims 3, 5, 21, and 23, Applicant respectfully disagrees with the Examiner with respect to the art as applied, but in light of claims 3, 5, 21, and 23 depending from what are believed otherwise allowable claims, Applicant does not believe additional

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remarks are necessary and requests allowance of claims 3, 5, 21, and 23 based on the chain of dependency.

Therefore, in light of at least the foregoing, Applicant respectfully believes that the present application is in condition for allowance. As a result, Applicant respectfully requests timely issuance of a Notice of Allowance for claims 1-6, 17-19, and 21-24.

Applicant appreciates the Examiner's consideration of these Amendments and Remarks and cordially invites the Examiner to call the undersigned, should the Examiner consider any matters unresolved.

Respectfully submitted,

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Dated: December 19, 2005
Attorney Docket No.: ITW7510.056

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